Amendments to the Specification (other than claims):

Please replace paragraph [0007] with the following amended paragraph:

[0007] Scaling-up of semiconductor substrates has been moving forward in recent years, however. For example, with silicon (Si) wafers, a transition from 8-inch to 12-inch is in progress. Consequent on this ~~impressive diametric~~ enlarging in diametric span of the semiconductor substrate, that the temperature distribution in the heating surface (retaining surface) of semiconductor substrates on ceramic susceptors be within [[Â±1.0%]] ±1.0% has become a necessity; that it be within [[Â±0.5%]] ±0.5% has, moreover, become an expectation.

Please replace paragraph [0015] with the following amended paragraph:

[0015] The present inventors discovered that in order to get the temperature distribution in the wafer-retaining surface to be within [[Â±1.0%]] ±1.0%, the spacing between the electrodes connected to the wafer holder should be 10% or more of the wafer holder thickness. A wafer undergoes predetermined processes with the wafer holder heating the wafer by means of a heating element formed either in the interior of the wafer holder, or else on a surface other than its wafer-carrying surface. But because heat escapes from the electrodes for electrically feeding the wafer holder circuits such as the heating element, there is a tendency for the temperature of the areas in the wafer-carrying surface that correspond to where the electrodes are furnished to drop. The tendency for the temperature to drop becomes especially pronounced in cases where numerous electrodes are clustered. The fact the temperature of the wafer being carried will drop sporadically if the temperature of the wafer-carrying surface drops sporadically will for example create fluctuations in the thickness and properties of films formed when a film-forming process is conducted on the wafer. In etching processes, for example, fluctuations in etching speed will be produced.

Please replace paragraph [0016] with the following amended paragraph:

[0016] This is why as slight as possible a temperature distribution in the wafer-carrying surface—currently, an isothermal rating of within [[Å±1.0%]] ±1.0%, with expectations for an isothermal rating of within [[Å±0.5%]] ±0.5% likely—is being sought. It was discovered that in order to gain an isothermal rating along these lines, the inter-electrode spacing should be made 10% or more of the wafer holder thickness. This is because although the shorter the spacing between electrodes, the greater the influence on heat escape through the electrodes, if the wafer-carrying surface of the wafer holder is thick, the impact on heat escape can be mitigated.

Please replace paragraph [0017] with the following amended paragraph:

[0017] Reference is made to the figure as a more specific example, wherein an RF electrode circuit 2 and a heater circuit 3 are formed in a wafer holder 1, and electrodes 4 are connected to the respective circuits. The spacing [[*l*]] ℓ between electrodes 4 is made 10% or more of *t*, the thickness of the wafer holder 1. Herein, in cases like in the figure where the wafer holder has numerous electrodes, the narrowest inter-electrode interval is in the present invention taken to be the electrode spacing.

Please replace paragraph [0032] with the following amended paragraph:

[0032] Next, heating and degreasing processes are carried out on the molded mass within a non-oxidizing atmosphere. Carrying out the degreasing process under an oxidizing atmosphere such as air would degrade the thermal conductivity of the sinter, because the AlN powder would become superficially oxidized. Preferable non-oxidizing ambient gases are nitrogen and argon. The heating temperature in the degreasing process is preferably [[500 Å°C]] 500°C or more and [[1000 Å°C]]

1000°C or less. With temperatures of less than [[500 Â°C]] 500°C, surplus carbon is left remaining within the laminate following the degreasing process because the binder cannot sufficiently be eliminated, which interferes with sintering in the subsequent sintering step. On the other hand, at temperatures of more than [[1000 Â°C]] 1000°C, the ability to eliminate oxygen from the oxidized coating superficially present on the surface of the AlN powder deteriorates, such that the amount of carbon left remaining is too little, degrading the thermal conductivity of the sinter.

Please replace paragraph [0034] with the following amended paragraph:

[0034] Next, sintering is carried out. The sintering is carried out within a non-oxidizing nitrogen, argon, or like atmosphere, at a temperature of 1700 to [[2000 Â°C]] 2000°C. Therein the moisture contained in the ambient gas such as nitrogen that is employed is preferably [[â□ì30 Â°C]] −30°C or less given in dew point. If it were to contain more moisture than this, the thermal conductivity of the sinter would likely be degraded, because the AlN would react with the moisture within the ambient gas during sintering and form nitrides. Another preferable condition is that the volume of oxygen within the ambient gas be 0.001 vol. % or less. A larger volume of oxygen would lead to a likelihood that the AlN would oxidize, impairing the sinter thermal conductivity.

Please replace paragraph [0036] with the following amended paragraph:

[0036] The obtained sinter is subjected to processing according to requirements. In cases where a conductive paste is to be screen-printed onto the sinter in a succeeding step, the surface roughness is preferably [[5 /1;4 m]] 5 μm or less in Ra. If over [[5 /1;4 m]] 5 μm, in screen printing to form circuits, defects such as blotting or pinholes in the pattern are liable to arise. More suitable is a surface roughness of [[1 /1;4 m]] 1 μm or less in Ra.

Please replace paragraph [0041] with the following amended paragraph:

[0041] The thickness of the conductive paste is preferably [[5 /1;4 m]] 5 μm or more and [[100 /1;4 m]] 100 μm or less in terms of it post-drying thickness. If the thickness were less than [[5 /1;4 m]] 5 μm the electrical resistance would be too high and the bonding strength decline. Likewise, if in excess of [[100 /1;4 m]] 100 μm the bonding strength would deteriorate in that case too.

Please replace paragraph [0042] with the following amended paragraph:

[0042] Also preferable is that in the patterns for the circuits that are formed, in the case of the heater circuit (resistive heating element circuit), the pattern spacing be 0.1 mm or more. With a spacing of less than 0.1 mm, shorting will occur when current flows in the resistive heating element and, depending on the applied voltage and the temperature, leakage current is generated. Particularly in cases where the circuit is employed at temperatures of [[500 Â°C]] 500°C or more, the pattern spacing preferably should be 1 mm or more; more preferable still is that it be 3 mm or more.

Please replace paragraph [0043] with the following amended paragraph:

[0043] After the conductive paste is degreased, baking follows. Degreasing is carried out within a non-oxidizing nitrogen, argon, or like atmosphere. The degreasing temperature is preferably [[500 Â°C]] 500°C or more. At less than [[500 Â°C]] 500°C, elimination of the binder from the conductive paste is inadequate, leaving behind carbon in the metal layer that during baking will form carbides with the metal and consequently raise the electrical resistance of the metal layer.

Please replace paragraph [0044] with the following amended paragraph:

[0044] The baking is suitably done within a non-oxidizing nitrogen, argon, or like atmosphere at a temperature of [[1500 Å°C]] 1500°C or more. At temperatures of less than [[1500 Å°C]] 1500°C, the post-baking electrical resistance of the metal layer turns out too high because the baking of the metal powder within the paste does not proceed to the grain growth stage. A further baking parameter is that the baking temperature should not surpass the firing temperature of the ceramic produced. If the conductive paste is baked at a temperature beyond the firing temperature of the ceramic, dispersive volatilization of the sintering promoter incorporated within the ceramic sets in, and moreover, grain growth in the metal powder within the conductive paste is accelerated, impairing the bonding strength between the ceramic and the metal layer.

Please replace paragraph [0046] with the following amended paragraph:

[0046] In that case, the amount of sintering promoter added preferably is 0.01 wt. % or more. With an amount less than 0.01 wt. % the insulative coating does not densify, making it difficult to secure electrical isolation of the metal layer. It is further preferable that the amount of sintering promoter not exceed 20 wt. %. Surpassing 30 wt. % leads to excess sintering promoter invading the metal layer, which can end up altering the metal-layer electrical resistance. Although not particularly limited, the spreading thickness preferably is [[5 /1;4 m]] 5 μm or more. This is because securing electrical isolation proves to be problematic at less than [[5 /1;4 m]] 5 μm.

Please replace paragraph [0047] with the following amended paragraph:

[0047] Further according to the present method, the ceramic as substrates can be laminated according to requirements. Lamination may be done via an adhesive agent. The adhesive agent—being a compound of Group IIa or Group IIIa elements,

and a binder and solvent, added to an aluminum oxide powder or aluminum nitride powder and made into a paste—is spread onto the bonding surface by a technique such as screen printing. The thickness of the applied adhesive agent is not particularly restricted, but preferably is [[5 /1;4 m]] 5 μm or more. Bonding defects such as pinholes and bonding irregularities are liable to arise in the adhesive layer with thicknesses of less than [[5 /1;4 m]] 5 μm.

Please replace paragraph [0048] with the following amended paragraph:

[0048] The ceramic substrates onto which the adhesive agent has been spread are degreased within a non-oxidizing atmosphere at a temperature of [[500 Â°C]] 500°C or more. The ceramic substrates are thereafter bonded to one another by stacking the ceramic substrates together, applying a predetermined load to the stack, and heating it within a non-oxidizing atmosphere. The load preferably is 0.05 kg/cm^2 or more. With loads of less than 0.05 kg/cm^2 sufficient adhesive strength will not be obtained, and otherwise defects in the joint will likely occur.

Please replace paragraph [0049] with the following amended paragraph:

[0049] Although the heating temperature for bonding is not particularly restricted as long as it is a temperature at which the ceramic substrates adequately bond to one another via the adhesive layers, preferably it is [[1500 Â°C]] 1500°C or more. At less than [[1500 Â°C]] 1500°C adequate adhesive strength proves difficult to gain, such that defects in the bond are liable to arise. Nitrogen or argon is preferably employed for the non-oxidizing atmosphere during the degreasing and boding just discussed.

Please replace paragraph [0054] with the following amended paragraph:

[0054] Subsequently, sheets that have undergone circuit formation are laminated with sheets that have not. Lamination is by setting the sheets each into position to

stack them together. Therein, according to requirements, a solvent is spread on between sheets. In the stacked state, the sheets are heated as may be necessary. In cases where the stack is heated, the heating temperature is preferably [[150 Â°C]] 150°C or less. Heating to temperatures in excess of this greatly deforms the laminated sheets. Pressure is then applied to the stacked-together sheets to unitize them. The applied pressure is preferably within a range of from 1 to 100 MPa. At pressures less than 1 MPa, the sheets are not adequately unitized and can peel apart during subsequent processes. Likewise, if pressure in excess of 100 MPa is applied, the extent to which the sheets deform becomes too great.

Please replace paragraph [0057] with the following amended paragraph:

[0057] A further preferable condition is that the surface roughness of the wafer-carrying surface be [[5 /1;4 m]] 5 μm in Ra. If the roughness is over [[5 /1;4 m]] 5 μm in Ra, grains loosened from the AlN due to friction between the wafer holder and the wafer can grow numerous. Particles loosened in that case become contaminants that have a negative effect on processes, such as film deposition and etching, on the wafer. Furthermore, then, a surface roughness of [[1 /1;4 m]] 1 μm or less in Ra is ideal.

Please replace paragraph [0058] with the following amended paragraph:

[0058] A wafer holder base part can thus be fabricated as in the foregoing. A shaft may be attached to the wafer holder as needed. Although the shaft substance is not particularly limited as long as its thermal expansion coefficient is not appreciably different from that of the wafer-holder ceramic, the difference in thermal expansion coefficient between the shaft substance and the wafer holder preferably is [[5 Â□$10^{Â-6}$K]] 5×10^{-6} K or less.

Please replace paragraph [0059] with the following amended paragraph:

[0059] If the difference in thermal expansion coefficient exceeds [[5 Å□$10^{Å-6}$K]] 5×10^{-6} K, cracks can arise adjacent the joint between the wafer holder and the shaft when it is being attached; but even if cracks do not arise when the two are joined, splitting and cracking can occur in the joint in that it is put through heating cycling in the course of being repeatedly used. For cases in which the wafer holder is AlN, for example, the shaft substance is optimally AlN; but silicon nitride, silicon carbide, or mullite can be used.

Please replace paragraph [0061] with the following amended paragraph:

[0061] The planarity of the respective joining faces of the shaft and wafer holder to be joined preferably is 0.5 mm or less. Planarity greater than this makes gaps liable to occur in the joining faces, impeding the production of a joint having adequate gastightness. A planarity of 0.1 mm or less is more suitable. Here, still more suitable is a planarity of the wafer holder joining faces of 0.02 mm or less. Likewise, the surface of the respective joining faces preferably is [[5 /1;4 m]] 5 μm or less in Ra. Surface roughness exceeding this would then also mean that gaps are liable to occur in the joining faces. A surface roughness of [[1 /1;4 m]] 1 μm or less in Ra is still more suitable.

Please replace paragraph [0066] with the following amended paragraph:

[0066] 99 parts by weight aluminum nitride powder and 1 part by weight Y_2O_3 powder were mixed and blended with 10 parts by weight polyvinyl butyral as a binder and 5 parts by weight dibutyl phthalate as a solvent, and doctor-bladed into a green sheet 430 mm in diameter and 1.0 mm in thickness. Here, an aluminum nitride powder having a mean particle diameter of [[0.6 /1;4 m]] 0.6 μm and a specific surface area of 3.4 m^2/g was utilized. In addition, a tungsten paste was prepared

utilizing 100 parts by weight of a tungsten powder whose mean particle diameter was [[2.0 /1;4 m]] 2.0 μm; and per that, 1 part by weight Y_2O_3 and 5 parts by weight ethyl cellulose, being a binder; and butyl [[Carbitolâ]] Carbitol™ as a solvent. A pot mill and a triple-roller mill were used for mixing. This tungsten paste was formed into a heater circuit pattern by screen-printing onto the green sheet.

Please replace paragraph [0067] with the following amended paragraph:

[0067] Pluralities of separate green sheets of thickness 1.0 mm were laminated onto the green sheet printed with the heater circuit to create laminates whose total thickness was in three thickness categories. Lamination was carried out by stacking the sheets in place in a mold, and thermopressing 2 minutes in a press at a pressure of 10 MPa while maintaining [[50Å°C]] 50°C heat. The laminates were thereafter degreased within a nitrogen atmosphere at [[600 Å°C]] 600°C, and sintered within a nitrogen atmosphere under time and temperature conditions of 3 hours and [[1800 Å°C]] 1800°C, whereby wafer holders of the three thickness categories were produced. Here, a polishing process was performed on the wafer-carrying surfaces so that they would be [[1 /1; 4 m]] 1 μm or less in Ra. The post-processing thicknesses of the sintered laminates were rendered into three categories: 5, 10 and 20 mm.

Please replace paragraph [0068] with the following amended paragraph:

[0068] The heater circuits in the wafer holders were partially exposed by spot-facing through the surface in two locations on the side opposite the wafer-carrying surface, up to the heater circuit. At this time, test samples in which the separation between the two locations differed, i.e., in which the inter-electrode spacing differed, were prepared. Electrodes made of tungsten were connected directly to the exposed portions of the heater circuits utilizing an active metal brazing material. The wafer holders were heated by passing current through the electrodes, and their isothermal

ratings were measured. Measurement of isothermal ratings was by setting a 12-inch wafer temperature gauge on the wafer-carrying surfaces and measuring their temperature distributions. It should be understood that the power supply was adjusted so that the temperature in the midportion of the wafer temperature gauge would be [[550 Å°C]] 550°C. The results are set forth in the table. Here, the proportional relation between the thickness of the wafer holders and the inter-electrode spacing (inter-electrode spacing/wafer-holder thickness) is given in the table.

Please delete paragraph [0069].

Please replace paragraph [0070] with the following amended paragraph:

[0070] Table.

No.	Wafer holder thickness (mm)	Inter-electrode spacing (mm)	Percentage (%)	Isothermal rating (%)
1	5	0.2	4	[[Å ± 1.3]] ± 1.3
2	5	0.4	8	[[Å ± 1.1]] ± 1.1
3	5	0.5	10	[[Å ± 0.8]] ± 0.8
4	5	1.0	20	[[Å ± 0.5]] ± 0.5
5	5	2.0	40	[[Å ± 0.4]] ± 0.4
6	10	0.5	5	[[Å ± 1.2]] ± 1.2
7	10	1.0	10	[[Å ± 0.7]] ± 0.7
8	10	2.0	20	[[Å ± 0.5]] ± 0.5
9	10	4.0	40	[[Å ± 0.4]] ± 0.4
10	20	1.0	5	[[Å ± 1.1]] ± 1.1
11	20	2.0	10	[[Å ± 0.6]] ± 0.6
12	20	4.0	20	[[Å ± 0.4]] ± 0.4
13	20	8.0	40	[[Å ± 0.3]] ± 0.3

Please replace paragraph [0071] with the following amended paragraph:

[0071] As is evident from the table, by making the inter-electrode spacing 10% or more of the thickness of the wafer holders, the temperature distribution in the wafer-carrying surface could be brought within [[Â± 1%]] ± 1%. What is more, making the inter-electrode spacing 10% or more of the thickness of the wafer holders can bring the temperature distribution in the wafer-carrying surface within [[Â± 0.5%]] ± 0.5%.